REMARKS

Claims 1-14, 22-32, and 39-42 are pending. Claims 1, 7, 23, and 25 are the remaining independent claims under consideration.

CLAIM 1

In the action mailed March 22, 2006, claim 1 was rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,289,473 to Takase (hereinafter "Takase"). Claim 1 was also rejected under 35 U.S.C § 103(a) as obvious over Takase and U.S. Patent No. 4,502,116 to Fowler et al. (hereinafter "Fowler").

As amended, claim 1 relates to a method that includes receiving an indication that a first peripheral is to participate in an execution of a breakpoint whereas a second peripheral is not to participate, in response to a first signal indicating that a processor has encountered the breakpoint, suspending execution of the first peripheral and saving the state of the first peripheral, continuing execution of the breakpoint by the processor and the first peripheral in response to receiving a second signal indicating that the state of the first peripheral has been saved, and restoring the saved state of the first peripheral in response to a third signal indicating that execution of the breakpoint by the processor has been completed.

Takase neither describes nor suggests receiving an indication that a first peripheral is to participate in an execution of a breakpoint whereas a second peripheral is not to participate, as recited in claim 1.

In this regard, Takase describes an audio image processor that includes a CPU 11 and various modules 12, 13, 14 that are under the control of a debug control circuit 17. *See Takase*, FIG. 1 and the written description thereof. In the implementation shown in Takase's FIG. 2, the states of CPU 11 and various modules 12, 13, 14 (on signal lines S11, S12, S13, S14) are treated identically, as indicated by uniform handling by OR-gates G1, G2, G3 and AND-gate G4. Thus, Takase's FIG. 2 neither describes nor suggests that an indication that a first peripheral is to participate in an execution of a breakpoint whereas a second peripheral is not to participate is received, as recited in claim 1.

However, Takase also describes that debug control circuit 17 can include the logic operation circuit 19 of FIG. 6 to change the output of debug control circuit 17 in accordance with "a combination of a state of a module." *See Takase*, col. 14, line 19-24. Please note that logic operation circuit 19 can replace any of OR-Gates G1, G2, G3 shown in FIG. 2. *See Takase*, FIG. 5; col. 15, line 24-28 (describing that "more complicated

arm conditions and disarm conditions can be processed" with logical operation circuit 19 in place of OR gates G1 and G2.) With such a replacement, the contents of logical value setting register 192 can be EXNOR'ed with selected signal S11, S12, S13 to "deal with various debug patterns." *See Takase*, FIG. 6; col. 15, line 1-12.

To determine the debug patterns that can be achieved with logical operation circuit 19, applicant submits that the information content of signal lines S11, S12, S13 is relevant. For example, trigger condition signal S13 is output from each module when a predetermined specific event (i.e., a "trigger condition") is generated in the module. *See Takase*, col. 6, line 56-61. Thus, trigger condition signal S13 indicates that a module has reached a trigger, and logical value setting register 192 allows reaching a trigger by some modules to have a different impact than other modules.

Applicant submits that changing the impact of a module reaching a trigger does not describe or suggest changing whether or not the module is to participate in an execution of a breakpoint Accordingly, the replacement of OR-Gate G3 with logic operation circuit 19 neither describes nor suggests that an indication that a first peripheral is to participate in an

execution of a breakpoint whereas a second peripheral is not to participate is received, as recited in claim 1

Arm condition signal S11 permits a stop signal S1 to be changed when the trigger condition signal S13 is changed. In other words, the arm condition signal S11 is a "trigger condition accepting signal" that allows the trigger condition indicated by S13 to be accepted. *See Takase*, col. 6, line 66-col. 7, line 7.

Applicant submits that changing whether or not a module can allow a trigger condition to be accepted does not describe or suggest changing whether or not the module is to participate in an execution of a breakpoint Accordingly, the replacement of OR-Gate G1 with logic operation circuit 19 neither describes nor suggests that an indication that a first peripheral is to participate in an execution of a breakpoint whereas a second peripheral is not to participate is received, as recited in claim 1.

Disarm condition signal S12 negates a change to stop signal S1 even if the trigger condition signal S13 is changed. In other words, the disarm condition signal S12 is a "trigger condition excluding signal."

Applicant submits that changing whether or not a module can exclude a trigger condition does not describe or suggest

changing whether or not the module is to participate in an execution of a breakpoint Accordingly, the replacement of OR-Gate G2 with logic operation circuit 19 neither describes nor suggests that an indication that a first peripheral is to participate in an execution of a breakpoint whereas a second peripheral is not to participate is received, as recited in claim 1.

Thus, neither Takase's FIG. 2 nor the embodiments that include logic operation circuit 19 describe nor suggest that an indication that a first peripheral is to participate in an execution of a breakpoint whereas a second peripheral is not to participate is received, as recited in claim 1. Claim 1 is thus not anticipated by Takase.

Fowler does not remedy this deficiency in Takase. In this regard, Fowler specifies that his interface circuit handles four different types of signals, i.e., pause-in signals, pause-out signals, resume-in signals, and resume-out signals. None of these signals indicates that a first peripheral is to participate in an execution of a breakpoint whereas a second peripheral is not to participate, as recited in claim 1. Fowler thus shares the same deficiency as Takase.

Claim 1 is thus not obvious over Fowler and Takase. Applicant respectfully requests that the anticipation and

obviousness rejections of claim 1 and the claims dependent therefrom be withdrawn.

CLAIM 7

Claim 7 was rejected under 35 U.S.C. § 102(b) as anticipated by Takase. Claim 7 was also rejected under 35 U.S.C. § 103(a) as obvious over Takase and Fowler.

As amended, claim 7 relates to a system that includes a processor, a first computer-readable medium storing instructions, a second computer-readable medium storing instructions, a first peripheral coupled to the processor, a second peripheral coupled to the processor, and a digital logic circuit comprising a memory that stores an indicator indicating that the first peripheral is to participate in an execution of the breakpoint but the second peripheral is not to participate. The digital logic circuit is coupled to the processor, the first peripheral, and the second peripheral.

Takase neither describes nor suggests a digital logic circuit comprising a memory that stores an indicator indicating that the first peripheral is to participate in an execution of the breakpoint but the second peripheral is not to participate, as recited in claim 7.

In this regard, as discussed above, neither Takase's FIG. 2 nor the embodiments that include logic operation circuit 19 describe nor suggest a situation where the first peripheral could participate in an execution of the breakpoint whereas a second peripheral would not participate. Accordingly, Takase neither describes nor suggests a memory that stores an indicator, as recited in claim 7. Claim 7 is thus not anticipated by Takase.

Fowler does not remedy this deficiency in Takase. In this regard, Fowler specifies that his interface circuit handles four different types of signals, i.e., pause-in signals, pause-out signals, resume-in signals, and resume-out signals. None of these signals indicates that a first peripheral is to participate in an execution of a breakpoint whereas a second peripheral is not to participate, as recited in claim 7. Fowler thus shares the same deficiency as Takase.

Claim 7 is thus not obvious over Fowler and Takase. Applicant respectfully requests that the anticipation and obviousness rejections of claim 7 and the claims dependent therefrom be withdrawn.

CLAIM 23

Claim 23 was rejected under 35 U.S.C. § 102(b) as anticipated by Takase. Claim 23 was also rejected under 35 U.S.C. § 103(a) as obvious over Takase and Fowler.

As amended, claim 23 relates to an apparatus that includes one or more signal lines used to receive signals and to send signals, a first processor; a second processor; a third processor, and a memory to store an indicator indicating that the second processor is to participate in an execution of a breakpoint but the third processor is not to participate in the execution.

Takase neither describes nor suggests a memory to store an indicator indicating that the second processor is to participate in an execution of a breakpoint but the third processor is not to participate in the execution, as recited in claim 23.

In this regard, as discussed above, neither Takase's FIG. 2 nor the embodiments that include logic operation circuit 19 describe nor suggest a situation where one processor could participate in an execution of the breakpoint whereas a second processor would not participate. Accordingly, Takase neither describes nor suggests a memory that stores an indicator, as recited in claim 23. Claim 23 is thus not anticipated by Takase.

Fowler does not remedy this deficiency in Takase. In this regard, Fowler specifies that his interface circuit handles four different types of signals, i.e., pause-in signals, pause-out signals, resume-in signals, and resume-out signals. None of these signals indicates that a second processor is to participate in an execution of a breakpoint but a third processor is not to participate in the execution, as recited in claim 23. Fowler thus shares the same deficiency as Takase.

Claim 23 is thus not obvious over Fowler and Takase. Applicant respectfully requests that the anticipation and obviousness rejections of claim 23 and the claims dependent therefrom be withdrawn.

CLAIM 25

Claim 25 was rejected under 35 U.S.C. § 102(b) as anticipated by Takase. Claim 25 was also rejected under 35 U.S.C. § 103(a) as obvious over Takase and Fowler.

As amended, claim 25 relates to an apparatus that includes one or more signal lines used to receive signals and to send signals, a first peripheral configured to: suspend execution and save a state of the first peripheral, a second peripheral, and a memory to store an indicator indicating that the first peripheral is to participate in the execution of the breakpoint

but the second peripheral is not to participate in the execution.

Takase neither describes nor suggests a memory to store an indicator indicating that the first peripheral is to participate in the execution of the breakpoint but the second peripheral is not to participate in the execution, as recited in claim 25.

In this regard, as discussed above, neither Takase's FIG. 2 nor the embodiments that include logic operation circuit 19 describe nor suggest a situation where one peripheral could participate in an execution of the breakpoint whereas a second peripheral would not participate.

Accordingly, Takase neither describes nor suggests a memory that stores an indicator as recited in claim 25. Claim 25 is thus not anticipated by Takase.

Fowler does not remedy this deficiency in Takase. In this regard, Fowler specifies that his interface circuit handles four different types of signals, i.e., pause-in signals, pause-out signals, resume-in signals, and resume-out signals. None of these signals indicates that a first peripheral is to participate in the execution of a breakpoint but a second peripheral is not to participate in the execution, as recited in claim 25. Fowler thus shares the same deficiency as Takase.

Claim 25 is thus not obvious over Fowler and Takase. Applicant respectfully requests that the anticipation and obviousness rejections of claim 25 and the claims dependent therefrom be withdrawn.

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Attorney's Docket No.: 10559-515001/P12419
Intel Corporation

Applicant asks that all claims be allowed. Pursuant to 37 CFR §1.136, applicant hereby petitions that the period for response to the action dated March 22, 2006, be extended for one month to and including July 22, 2006.

Please charge the $120 Petition for Extension of Time fee to Deposit Account No. 06-1050. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: July 24, 2006

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